Literal support for the choice of wording is not required and support may be provided by the figures and what one of ordinary skill in the art would appreciate. At the time the application filed, one skilled in the art would understand a "wafer" to be an integrated circuit substrate. At the time the application was filed, one of ordinary skill in the art would appreciate the wafer 38 in Fig. 4 to be an integrated circuit substrate having a plurality of LED die formed thereon.

Accordingly, applicants submit that claim 21 is in proper form under 35 U.S.C. § 112, first paragraph because the specification satisfactorily conveys to one of ordinary skill in the art that the applicants were in possession of the invention as claimed, including a plurality of light emitting diode die formed on the integrated circuit substrate.

Claims 21-23, 25-27, and 29-31 are rejected under 35 U.S.C. § 102(e) as being anticipated by Ishinaga (U.S. Patent No. 6,093,940). Claims 24 and 28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ishinaga. Applicants respectfully traverse these rejection for the following reasons.

Claim 21 recites a surface mount light emitting diode package including a plurality of light emitting diode die formed on an integrated circuit substrate. Ishinaga fails to teach or suggest this recited claim feature.

In contrast to the invention as recited in claim 21, Ishinaga teaches only the conventional arrangement, wherein a plurality of separate LED die are utilized in an LED package. Substrate 1 is not an integrated circuit substrate, as that term would be understood in the art. Rather, substrate 1 would be considered a packaging substrate.

Moreover, the two LEDs in Ishinaga are not formed on the substrate 1, rather they are affixed to the substrate 1. Ishinaga discloses that "the two LED elements 2a and 2b are individually fixed" on the substrate (see col. 1, lines 35-37).

As noted in the specification, there are numerous cost and manufacturing advantages to the device structure recited in claim 21. None of these cost or manufacturing advantages are taught or suggested by Ishinaga.

Because Ishinaga fails to teach or suggest a surface mount light emitting diode package including a plurality of light emitting diode die formed on an integrated circuit

substrate, claim 21 and its dependent claims are not anticipated by and are patentable over Ishinaga.

Claim 25 recites a surface mount light emitting diode package including a plurality of LED die which comprise integrally connected adjacent die from a single wafer. For the reasons given above, the die disclosed in Ishinaga are not integrally connected, are not adjacent, and do not come from a single wafer. Accordingly, the § 102 rejection must be withdrawn. Moreover, as noted in the specification, there are numerous cost and manufacturing advantages to the device structure recited in claim 25. None of these cost or manufacturing advantages are taught or suggested by Ishinaga.

Applicants do not understand the Examiner's statement on page 3, lines 10-11 that "a die inherently form a single wafer;" Assuming the Examiner means die "from" a single wafer, this is not inherent because the conventional arrangement may utilize die from different wafers.

With respect to paragraph 6 of the office action, the Examiner's argument is not understood because there are no product-by-process claims pending in the present application. The recitation "adjacent die from a single wafer" describes a structural relationship, not a process.

In fact, Ishinaga teaches away from using a plurality of die from the same substrate. Ishinaga is directed to a two color LED package which uses two different color LED elements (2a is red and 2b is green, see col. 1, lines 65-67). Accordingly, the two die 2a and 2b do not come from the same substrate.

With respect to paragraph 13, the office action asserts that applicant has not established a prima facie that dies from a single wafer cannot have different colors. However, applicant has no such burden. It is well established law that applicants are entitled to their patent unless the Patent Office establishes evidence to the contrary. Applicants note that the publication US 20020030444 cited for support for the Examiner's position that "LEDs of same wafer that emit different color" is not properly of record in this case. In any event, the Examiner misconstrues the publication, which merely describes that an underlying wafer may be processed to deposit thin films on the wafer which change the color emitted by the LEDs on the wafer. However, all die from

the processed wafer emit the same color (in fact uniformity in color appears to be the object of the publication).

Applicants disagree with the Examiner's assertion that "adjacent die from a single wafer" does not describe a structural relationship except that the LED has a substrate. First the Examiner ignores the language "integrally connected" which further describes the structural relationship. Taken as whole, one of ordinary skill in the art would understand the phrase to indicate two or more adjacent die from the same wafer which have not been cut or separated. It is improper for the Examiner to ignore the recited language or not give the language patentable weight.

Because Ishinaga fails to teach or suggest a surface mount light emitting diode package including a plurality of LED die which comprise integrally connected adjacent die from a single wafer, claim 25 and its dependent claims are not anticipated by and are patentable over Ishinaga.

With respect to paragraph 11 of the office action, the principle cited by the Examiner does not appear to have any bearing on the present application because the claims are not directed to a mere duplication of elements, but more particularly to a novel arrangement of elements, which the office action admits is not disclosed in the prior art.

Finally, with respect to paragraph 14 of the office action, the principle cited by the Examiner does not appear to have any bearing on the present application because the advantages provided by the present invention are simply not provided by any device described in Ishinaga. Moreover, the Examiner has not identified any suggestion of the prior art to "follow" from which the advantages would naturally flow. Applicants have not merely recognized another advantage provide by the device of Ishinaga. Rather, applicants have invented a new device which provides numerous cost and manufacturing advantages as compared to the device described by Ishinaga.

In view of the foregoing, favorable reconsideration and withdrawal of the rejections is respectfully requested. If the rejections are maintained, applicants respectfully request that the Examiner contact the undersigned attorney at the telephone number listed below to arrange a personal interview.

Respectfully submitted,

December 3, 2003
Date

Paul E. Steiner
Reg. No. 41,326
(703) 633 - 6830

Intel Americas
LF3
4030 Lafayette Center Drive
Chantilly, VA 20151

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